REMARKS

Applicants respectfully traverse and request reconsideration.

Claims 1, 4 and 17 stand rejected under 35 U.S.C. § 102(e) as being unpatentable over Lin, U.S. Patent No. 6,256,746 ("Lin"). Lin is directed at a system and method for reducing power consumption and heat dissipation of at least two functional units of a microelectronic device. Based on the strategy that all of the functional units on a single chip do not need to be operational at a given time in the execution of a computer program that is controlling the microelectronic device, Lin discloses a system and method for turning on and off a functional unit. In accordance with Figure 4, Lin discloses a logic unit (Element 116) responsive to a system clock (Element 104) and monitoring information from machine code instructions (Element 402). Monitoring information is provided to the logic unit in accordance with the systems and methods of Figure 6 and Figure 8. In both figures, a computer program in source code form is supplied to a compiler for compiling source code into machine code. With respect to Figure 6, compiler (Element 604) produces machine code instructions 606, 610, 614, 618, 622 and 626. Each machine code instruction has a corresponding functional unit data block, which constitutes the monitoring information that is supplied via a path (FIG. 4, Element 402) to the logic unit (FIG. 4, Element 116) In response to the functional unit data blocks, the logic unit can turn on and off various functional units by supplying a system clock signal (FIG. 4, Element 302) to the appropriate clock input line corresponding to the functional unit that is instructed to turn on. When that functional unit is to be turned off, the logic unit no longer provides the system clock signal along the input line. In this manner, the logic unit can control when a functional unit is turned on or off by either supplying or no longer supplying a clock signal to a particular functional unit. (Column 9, Lines 33-63; Column 10, Lines 31-43).

An alternative approach for turning on and off a functional unit is illustrated in Figure 5. In particular, Figure 5 includes a plurality of latches (Elements 504, 510, 516 and 522) that latch and hold a previous input value (Element 502). Latches are controlled to pass the input to a plurality of corresponding functional units based upon control lines (Elements 508, 514, 520 and 526) generated by the logic unit in accordance with monitoring information from machine code instructions (Element 402). In this manner, various functional units are turned on and off by controlling the state change of the inputs for these functional units. (Column 9, Line 64 - Column 10, Line 19).

With respect to Claim 1 and new Claim 20, Lin fails to disclose a power consumption reduction circuit comprising a memory clock source of a graphic controller; and a memory clock tree circuit of a graphics controller, operatively coupled to the memory clock source, that generates branches of memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for differing processing engines and selectively activates at least some of the plurality of independent clock signals in response to received condition data during an active mode. Lin is dedicated to a compiler system and discloses a system requiring a compiler and method whereby *compiled machine code instructions* from a compiler indicate which functional unit on a single microelectronic device are to be turned on or off. (Emphasis added). In response to machine code instructions, a logic unit provides a *system clock signal* on the appropriate clock input line for the functional unit that is to be turned on. (Emphasis Added).

Applicants respectfully submit that the system clock source and monitoring information from machine code instructions as taught by Lin are not analogous to a memory clock source of a graphics controller and received condition data as taught by Applicants. In reference to

Applicants' Figure 3, a memory clock source is operatively coupled to a memory clock tree circuit that generates branches of memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for different processing engines. *In response to received condition data*, the memory clock tree circuit selectively activates at least some of the plurality of independent clock signals. (Emphasis added). Independent clock signals selectively activated by the memory clock tree circuit are provided to a corresponding plurality of corresponding individual buffer circuits and memory request interfaces. As illustrated in Figure 3, the plurality of corresponding memory request interfaces activated by independent clock signals request data from a memory controller (Element 310). As such, the memory controller may utilize a power consumption reduction circuit as illustrated in Figure 2 to accept a memory read request signal and provide latched memory read data. In addition, an engine clock circuit (Fig. 3, Element 306) provides a *separate and distinct engine clock* signal to a plurality of requesters and engine blocks corresponding to memory request interfaces activated by the memory clock tree circuit. (Emphasis added).

In contrast to Applicants' memory clock source, a *system clock* (Fig. 4, Element 104) of Lin is directly provided to the plurality of functional units based on a compiler and *compiled machine code instructions*. (Emphasis added). The functional units provided with the system clock signal are operatively turned on for the duration of the system clock signal. Applicants' claimed invention is not responsive to compiled machine code instructions in the form of monitoring information, as taught by Lin; rather, the Applicants' claimed invention receives *condition data* during an active mode. (Emphasis added). Applicants' claimed invention operates using a memory clock and requires a memory clock tree circuit of a graphics controller. When read in light of the Specification, condition data may include, inter alia, data indicating

that a primary or secondary display has been selected, data indicating a graphic user interface engine is active, data indicating that video overlay scaler has been enabled, data indicating whether said picture operations have been enabled, and data indicating a video capture operation has been enabled. (Page 5, Lines 25-28). In summary, Lin discloses a compiler based system that uses a compiler to receive source code and compile to machine code instructions, and does not control a memory clock based on received condition data.

In light of above remarks, Applicants respectfully note that Lin fails to teach or disclose the limitations expressed in Applicants' Claim 1. Applicants respectfully believe Claim 1 is in proper condition for allowance.

With respect to Claim 4, the Applicants respectfully repeat the relevant remarks made in regard to Claim 1, and further submit that Claim 4 contains further patentable material. While Lin discloses a logic unit (FIG. 5, Element 116) and a plurality of latch circuits (FIG 5, Elements 504, 510, 516 and 522), Lin merely teaches an alternative approach for turning on and off the functional units. By not allowing the inputs of functional units to change state, a plurality of latches hold the previous inputs based upon control lines generated by a logic unit responsive to monitoring information from machine code instructions. (Col. 10, Lines 5-17). In contrast, the Applicants' Specification teaches a separate structure in which a plurality of *memory read latches* are dynamically activated and deactivated based on detected memory read requests to facilitate memory access activity based power reduction. (Emphasis Added). Specifically the memory read latch control circuit includes a read data latency compensation circuit which determines how long it takes for the memory to fetch data. The memory read latch control circuit includes control logic that receives the memory read request, obtains the read data latency information and generates a read latch control signal which indicates when to turn off the read

latching flops during an active mode to reduce power consumption. The memory read latch control circuit also includes an AND circuit responsive to the read latch control signal and also responsive to a memory clock signal generated by the memory clock source. The AND circuit selectively enables and disables the memory read latches by generating the enable signal as a function of the memory request. (Figure 2, Element 204; Page 6, Line 27-Page 7, Line 19). In addition, the Applicants teach a plurality of memory read latch circuits which receive memory data and are responsive to the memory read latch control circuit. As Lin fails to disclose the limitations of memory read latches and corresponding circuitry as set forth in Claim 4, the Applicants respectfully believe that Claim 4 is in proper condition for allowance.

With respect to Claim 7, the Applicants respectfully repeat the relevant remarks made above. In failing to disclose a power consumption reduction circuit comprising a memory clock tree circuit that selectively activates at least some of a plurality of independent clock signals in response to *receive condition data*, Lin also fails to disclose the subsequent claim limitations. In light of the above remarks, the Applicants respectfully believe that Claim 7 is in proper condition for allowance.

Claims 2 and 17-19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin. The Examiner has cited the system clock and logic unit (Figure 4, Elements 104 and 116, respectively) as teaching an engine clock source operatively coupled to a switching circuit that generates an output clock signal. The Applicants are confused to the Examiner's rejection of Claim 2 as the Examiner also cited the system clock of Claim 4 against the memory clock source of Applicants' Claim 1. The Applicants respectfully note that two clock sources, a memory clock source and a distinct engine clock source, are taught in Applicants' claimed invention. In contrast, the Lin reference only discloses one clock, namely a system clock. As such, the Lin

reference fails to disclose not only the memory clock source of Applicants' Claim 1, but also an engine clock.

Moreover, the inclusion of a video overlay engine, a video capture engine, an I2C control logic, a multimedia port, and video capture enable data in a power consumption reduction circuit such that the switching circuit disables the output clock signal based on condition data as listed in Claim 2 further distinguishes the Applicants' claimed invention from that of Lin. For example, Lin discloses a compiler-based system and is not directed to a graphics controller or video controller as taught in Applicants' Claims 1-2. Applicants respectfully request a showing of factual basis for the alleged motivation to include at least one of: video overlay engine, a video capture engine, an I2C control logic, a multimedia port, and video capture enable data in a power consumption reduction circuit. Furthermore, Applicants request the exact teaching that shows that such devices are "well known in the art of computer system[s]." (Office Action, Page 4, ¶ 12). Such a combination of devices included in the limitations of Applicants' Claim 2 with Lin would nevertheless result in a compiler-based video capture system not disclosed by Lin or other references or claimed by Applicants. Moreover, as Claim 2 inherits the limitations of Claim 1, Applicants respectfully believe Claim 2 is in proper condition for allowance.

With respect to Claims 17-19, the Applicants respectfully repeat the relevant remarks made above in regards to Claim 1. Specifically, the Lin reference fails to disclose the activation of a plurality of independent clock signals in response to *received condition data* during an active mode. As a result, the Lin reference furthermore fails to disclose any limitations upon said condition data. Claims 17-19 are respectively believed to be in proper condition for allowance.

Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin in view of Jones, Jr., U.S. Patent No. 5,781,768 ("Jones, Jr."). Jones, Jr. discloses a graphics controller utilizing a variable frequency clock. The system includes a memory clock for a graphics controller which includes a plurality of clock pulse generators, and a clock controller which selects the clock frequency based upon the state of the graphics controller functional units. (See Abstract). In Figure 4, Jones, Jr. shows clock control logic that generates control signals which act as select signals to select one of three different clock frequencies. Based on the state of the graphics controller functional units, the output of comparators 410, 411 and 412 are not independent clock signals divided from a memory clock but are control signals, one of which selects an appropriate clock frequency associated with CLK Select 430, CLK/2 Select 431 or CLK/4 Select 432. As such, the control signals selects one of three different clock frequencies as the memory clock frequency according to the table shown in Column 4. The Jones, Jr. reference is silent as to the limitations of Applicants' Claim 1. Furthermore, the Jones, Jr. reference fails to teach a circuit operative to vary the speed of a memory clock *based on a type of memory request from a plurality of memory requesters* as required in Claim 3. (Emphasis Added). Containing further patentable material, Applicants respectfully believe that Claim 3 is in proper condition for allowance.

Claims 5-6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin in view of Jones, Jr. and in further view of Houston, U.S. Patent No. 5,544,101 ("Houston"). The Applicants respectfully note that Claim 5 depends from allowable base Claim 4 while Claim 6 stems from Claim 5. Repeating the relevant remarks made with respect to Claims 1-4 (namely, Lin and Jones, Jr. not teaching a read data listing compensation circuit), the Applicants further note that Lin also fails to disclose a gating circuit responsive to the read latch control signal and a

memory clock signal operative to selectively enable and disable memory read latches as a function of memory requests.

Houston is directed to a memory device having a latching multiplexer and a multiplexer block therefor. The memory device includes a memory array, a multiplexer block and a control block. The memory array (FIG. 1, Element 12) provides a plurality of memory array outputs responsive to a memory address. Each memory array output represents a data state of a memory cell. The multiplexer block is coupled to the plurality of memory array outputs and provides a multiplexer block output representing a data state of a desired memory cell corresponding to the memory address responsive to a plurality of multiplexer control signals. The internal latch blocks are operable to receive a plurality of input signals, operable to retain a plurality of data states and operable to provide an output signal. (See Abstract). As stated in response to the Examiner's Advisory Action mailed August 27, 2002, this system is directed to circuits internal to memory, while the Applicants' memory latch circuits and control circuits are external to the memory device that receives the memory clock signal.. Instead, they are coupled to receive data from the memory device.

The Applicants respectfully assert that Houston fails to disclose any limitation of Claims 5-6. Moreover, the Applicants reassert the request to find factual support for the motivation to combine the teachings of Lin, Jones, Jr. and Houston. No combination of the three references teaches the limitations within the Applicants' claimed invention. The Applicants respectfully note that the basis of rejecting Claims 5-6 is little more than impermissible hindsight analysis. Per M.P.E.P. § 2142, the conclusion of obviousness "must be reached on the basis of the facts gleaned from the prior art." A conclusion of obviousness is proper "so long as it takes into account only knowledge which was within the level of ordinary skill in the art ...." (M.P.E.P. §

2145(X)(A)). In the instant case, the only apparent source of teaching of a memory read latch control circuit and the limitations inherent within Claims 5-6 is the instant Application. As such, the Applicants respectfully submit that Claims 5-6 are in proper condition for allowance.

Claims 8-9, 12-14 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin. With respect to Claim 8, the Applicants respectfully repeat the relevant remarks made in regard to Claims 1, 2 and 4 and again request a showing of where an engine clock and memory clock and control logic in a graphics controller are taught as claimed. With respect to Claim 9, the Applicants respectfully repeat the relevant remarks made in regard to Claim 3. With respect to Claim 12, the Applicants respectfully repeat the relevant remarks made in regard to Claim 7. Claims 13-14 and 16 represent the method claims of Claims 8-9 and 12. Applicants believe that Claims 8-9, 12 -14 and 16 are in proper condition for allowance.

Claims 10-11 and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin, in view of Jones, Jr. and further in view of Houston. With respect to Claim 10, the Applicants respectfully repeat the relevant remarks made in regard to Claim 5. With respect to Claim 11, the Applicants respectfully repeat the relevant remarks made in regard to Claim 6. Claim 15 represents the method claim of Claim 10. Applicants believe that Claims 10-11 and 15 are in proper condition for allowance.

Applicant respectfully submits that the claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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